REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27							
REV STATUS OF SHEETS				REV																
				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
96-07-31

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, MEMORY, FLASH ERASABLE/PROGRAMMABLE READ ONLY MEMORY, 512K x 32-BIT

SIZE	CAGE CODE	
A	**67268**	**5962-94612**

SHEET 1 OF 27

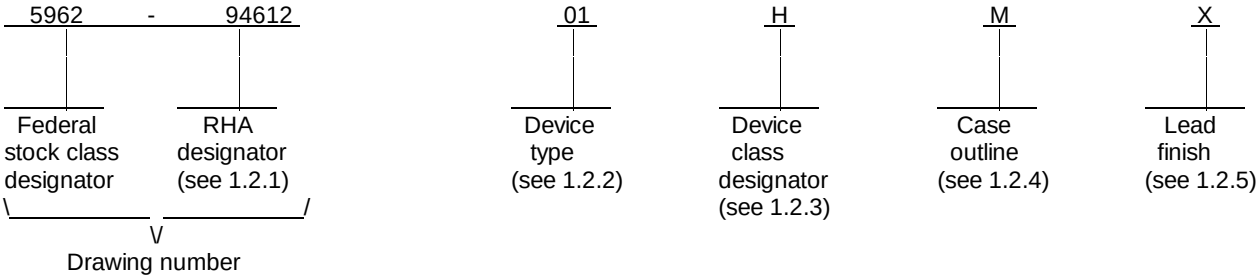
DESC FORM 193
JUL 94

5962-E422-96

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). This drawing describes device requirements for hybrid microcircuits to be processed in accordance with MIL-PRF-38534. Two product assurance classes, military high reliability (device class H) and space application (device class K) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number(PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes H and K RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	WF512K32-150, ACT-F512K32N-150	EPROM FLASH, 512K X 32-bit	150nS
02	WF512K32-120, ACT-F512K32N-120	EPROM FLASH, 512K X 32-bit	120nS
03	WF512K32-90, ACT-F512K32N-090	EPROM FLASH, 512K X 32-bit	90nS
04	WF512K32-70, ACT-F512K32N-070	EPROM FLASH, 512K X 32-bit	70nS

1.2.3 Device class designator. This device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
H or K	Certification and qualification to MIL-PRF-38534

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	See figure 1	68	Co-fired ceramic, single/dual cavity, quad flatpack
T	See figure 1	68	Co-fired ceramic, single cavity, low profile,quad flatpack
U	See figure 1	66	Co-fired ceramic, Hex-in-line, single cavity, with standoffs
N	See figure 1	68	Co-fired ceramic, single cavity, quad flatpack, low capacitance
X	See figure 1	66	Co-fired ceramic, Hex-in-line, single cavity, without standoffs

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534 for classes H and K. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-2.0 V dc to +7.0 V dc
Signal voltage range (V_G)(any pin except A9 2/)	-2.0 V dc to +7.0 V dc
Power dissipation (P_D)	1.32 W Max.at 5 MHz
Storage temperature range	-65° C to +150° C
Lead temperature (soldering, 10 seconds)	+300° C
Data retention	10 years minimum
Endurance (write/erase cycles)	10,000 cycles minimum
A9 voltage for sector protect (V_{ID})3/	-2.0 V dc to +14.0 V dc

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input low voltage range (V_{IL})	-0.5 V dc to +0.8 V dc
Input high voltage range (V_{IH})	+2.0 V dc to V_{CC} +0.5 V dc
Case operating temperature (T_C)	-55° C to +125° C
A9 voltage for sector protect	+11.5 V dc to +12.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbook. Unless otherwise specified, the following specification, standards, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

PERFORMANCE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input may overshoot V_{SS} to -2.0 V for periods of up to 20 nS. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods of up to 20 nS.
3/ Minimum DC input voltage on A9 pin is -0.5 V. During voltage transitions, A9 may overshoot V_{SS} to -2.0 V for periods of up to 20 nS. Maximum DC input voltage on A9 is +13.5 V which may overshoot to +14.0 V for periods of up to 20 nS.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38534 and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Timing diagram(s). The timing diagram(s) shall be as specified on figure 4, 5, and 6.

3.2.5 Block diagram(s). The block diagrams shall be as specified on figure 7.

3.2.6 Output load circuit. The output load circuit shall be as specified on figure 8.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Programming procedure. The programming procedure shall be as specified by the manufacturer and shall be available upon request.

3.6 Marking. Marking shall be in accordance with MIL-PRF-38534. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in QML-38534.

3.7 Manufacturer eligibility. In addition to the general requirements of MIL-PRF-38534, the manufacturer of the part described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, produced on the certified line, for each device type listed herein. The data should also include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.8 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance submitted to DSCC-VA shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38534 and the requirements herein.

3.9 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

3.10 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for the initial characterization and after any design process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

3.11 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC parameters							
Input leakage current	I_{LI}	V_{CC} = 5.5 Vdc, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
Output leakage current	I_{LO}	V_{CC} = 5.5 Vdc, V_{IN} = GND or V_{CC}	1,2,3	All		10	µA
V_{CC} active current for Read	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5 Vdc	1,2,3	All		190	mA
V_{CC} active current for program/erase	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5 Vdc	1,2,3	All		240	mA
V_{CC} standby current	I_{SB}	$\overline{CS}$ = V_{IH},f = 5MHz, V_{CC} = 5.5 Vdc	1,2,3	All		6.5	mA
Input low level	V_{IL}		1,2,3	All		0.8	V
Input high level	V_{IH}		1,2,3	All	2.0		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} =12.0 mA	1,2,3	All		0.45	V
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OL} =-2.5 mA	1,2,3	All	0.85 x V_{CC}		V
Dynamic characteristics							
$\overline{OE}$ capacitance 3/	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		50	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline N only	4	All		32	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55^\circ C \le T_C \le +125^\circ C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Dynamic characteristics- continued							
$\overline{WE}_{1-4}$ capacitance 3/	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outlines M and U	4	All		20	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline T	4	All		50	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline N	4	All		32	pF
$\overline{CS}_{1-4}$ capacitance 3/	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		20	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline N only	4	All		15	pF
Data I/O capacitance 3/	$C_{I/O}$	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		20	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline N only	4	All		15	pF
Address input 3/ capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C	4	All		50	pF
		V_{IN} = 0 V, f = 1.0 MHz T_A = +25° C Case outline N only	4	All		32	pF
Functional testing							
Functional tests		See 4.3.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle AC timing characteristics							
Read cycle time	t_{RC}	See figure 4	9,10,11	01 02 03 04	150 120 90 70		nS
Address access time	t_{ACC}	See figure 4	9,10,11	01 02 03 04		150 120 90 70	nS
Chip select access time	t_{CE}	See figure 4	9,10,11	01 02 03 04		150 120 90 70	nS
Output enable to output valid	t_{OE}	See figure 4	9,10,11	01 02 03,04		55 50 35	nS
Output hold from Address, CS or OE change, whichever is first	t_{OH}	See figure 4	9,10,11	All	0		nS
Write/Erase/Program AC timing characteristics $\overline{WE}$ controlled .							
Write Cycle time	t_{WC}	See figure 5	9,10,11	01 02 03 04	150 120 90 70		nS
Chip select setup time	t_{CS}	See figure 5	9,10,11	All	0		nS
Write enable pulse width	t_{WP}	See figure 5	9,10,11	01,02 03,04	50 45		nS

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/Program AC timing characteristics $\overline{WE}$ controlled - continued.							
Address setup time	t_{AS}	See figure 5	9,10,11	All	0		nS
Data setup time	t_{DS}	See figure 5	9,10,11	01,02 03,04	50 45		nS
Data hold time	t_{DH}	See figure 5	9,10,11	All	0		nS
Address hold time	t_{AH}	See figure 5	9,10,11	01,02 03,04	50 45		nS
Write enable pulse high	t_{WPH}	See figure 5	9,10,11	All	20		nS
Chip erase time			9,10,11	All		120	S
Sector erase time			9,10,11	All		30	S
Programming time			9,10,11	All		50	S
Write/Erase/Program AC timing characteristics $\overline{CS}$ controlled.							
Write cycle time	t_{WC}	See figure 6	9,10,11	01 02 03 04	150 120 90 70		nS
Write enable setup time	t_{WS}	See figure 6	9,10,11	All	0		nS
Chip select pulse width	t_{CP}	See figure 6	9,10,11	01,02 03,04	50 45		nS
Address setup time	t_{AS}	See figure 6	9,10,11	All	0		nS

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ 2/ $-55^{\circ}C \le T_C \le +125^{\circ}C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write/Erase/Program AC characteristics $\overline{CS}$ controlled.							
Data hold time	t_{DH}	See figure 6	9,10,11	All	0		nS
Data setup time	t_{DS}	See figure 6	9,10,11	01,02 03,04	50 45		nS
Address hold time	t_{AH}	See figure 6	9,10,11	01,02 03,04	50 45		nS
Chip select pulse width high	t_{CPH}	See figure 6	9,10,11	All	20		nS
Chip erase time			9,10,11	All		120	S
Sector erase time			9,10,11	All		30	S
Programming time			9,10,11	All		50	S

1/ Unless otherwise specified, $4.5\ V \le V_{CC} \le 5.5\ V$ and $V_{SS} = 0\ V$.

2/ Unless otherwise specified, the DC test conditions are as follows:
Input pulse levels: $V_{IH} = V_{CC} - 0.3\ V$ and $V_{IL} = 0.3V$.

Unless otherwise specified, the AC test conditions are as follows:
Input pulse levels: $V_{IL} = 0\ V$ and $V_{IH} = 3.0\ V$.
Input rise and fall times: 5 nanoseconds.
Input and output timing reference levels: 1.5 V.
Output load circuit as specified in figure 7.

3/ Parameters shall be tested as part of design characterization and after any design or process changes which may affect these parameters. Parameters shall be guaranteed to the limits specified in table I for all lots not specifically tested.

Case outline M

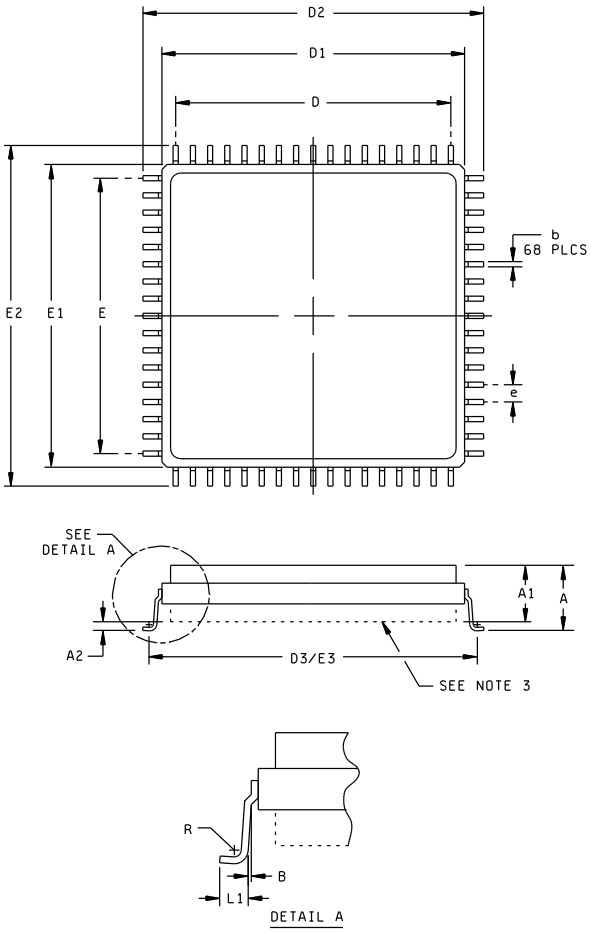


FIGURE 1. Case outlines.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.12	5.10	0.123	0.200
A1	2.30	4.72	0.118	0.186
A2	0.24	0.38	0.005	0.015
b	0.33	0.43	0.013	0.017
D/E	20.3 BSC		0.800 BSC	
D1/E1	22.10	22.65	0.870	0.890
D2/E2	24.89	25.35	0.980	1.000
D3/E3	23.75	24.28	0.936	0.956
e	1.27 BSC		0.050 BSC	
R	0.25 TYP.		0.010 BSC	
L1	0.89	1.14	0.035	0.045

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.
3. Case outline M may be either a single cavity or dual cavity package.

FIGURE 1. Case outlines- Continued.

Case outline N

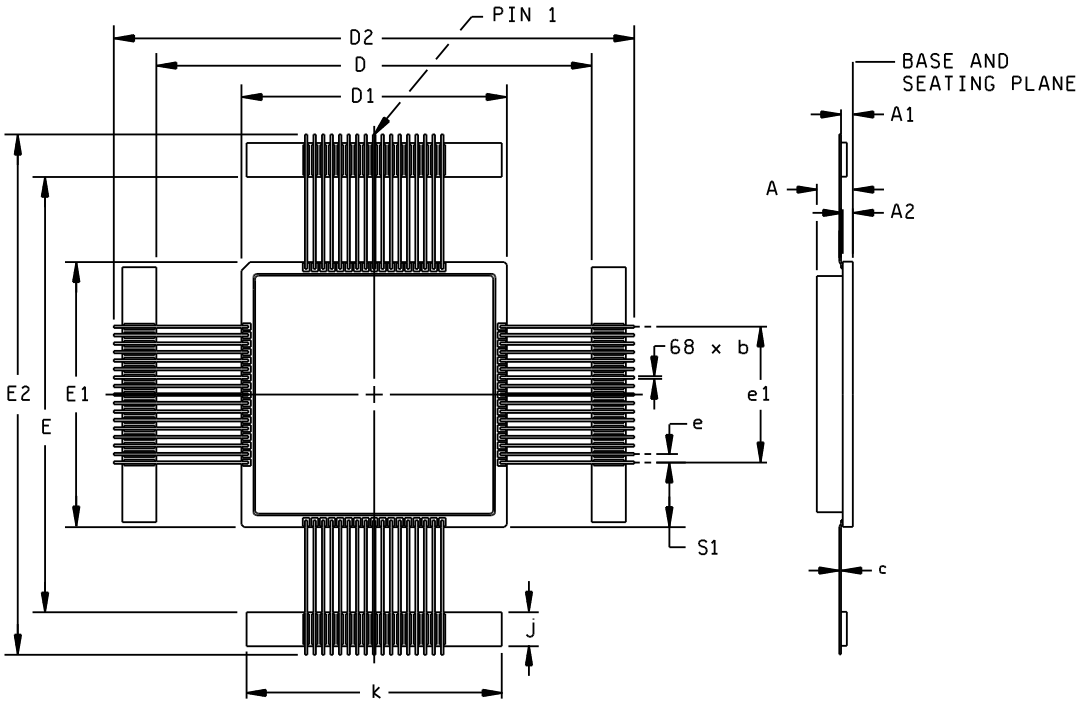


FIGURE 1. Case outlines - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	4.46	5.10	0.175	0.200
A1	1.40	1.65	0.055	0.065
A2	1.14	1.40	0.045	0.055
b	0.30	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	84.20	2.885	3.315
e	1.14	1.40	0.045	0.055
e1	19.10	21.16	0.750	0.850
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	0.480	0.520
S1	9.45	9.86	0.372	0.388

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outline T

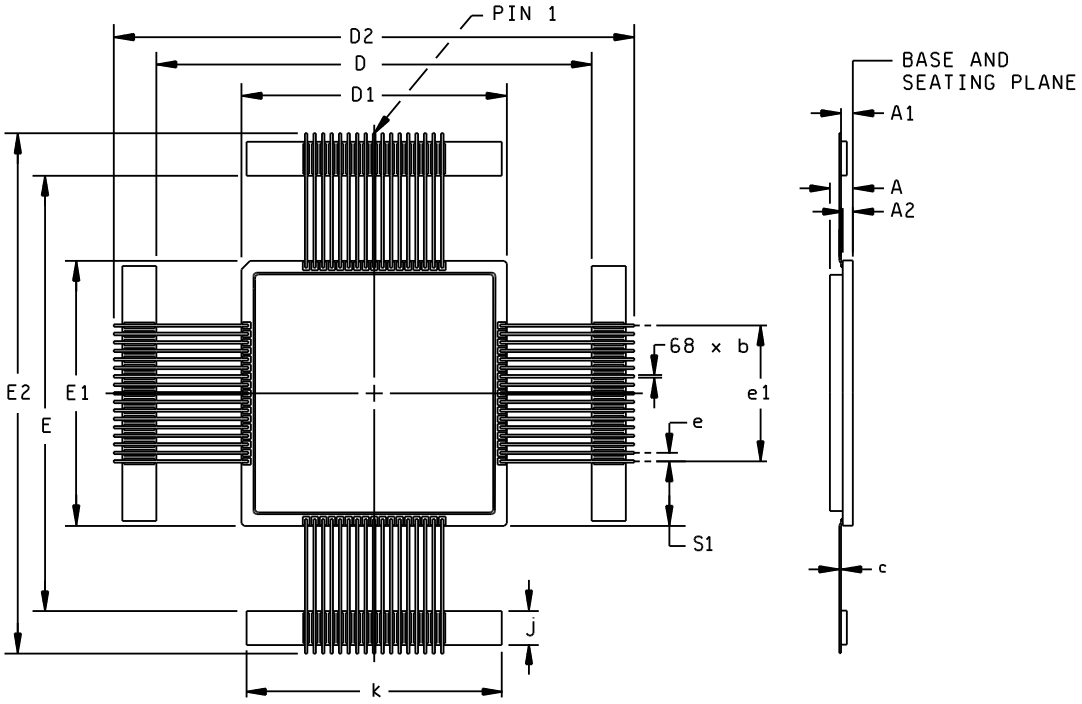


FIGURE 1. Case outlines - Continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	3.56	0.115	0.140
A1	1.40	1.65	0.055	0.065
A2	1.14	1.40	0.045	0.055
b	0.30	0.46	0.012	0.018
C	0.23	0.31	0.009	0.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	73.28	84.20	2.885	3.315
e	1.14	1.40	0.045	0.055
e1	19.10	21.16	0.750	0.850
j	4.83	5.33	0.190	0.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	0.480	0.520
S1	9.45	9.86	0.372	0.388

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin numbers are for reference only.

FIGURE 1. Case outlines - Continued.

Case outlines U and X

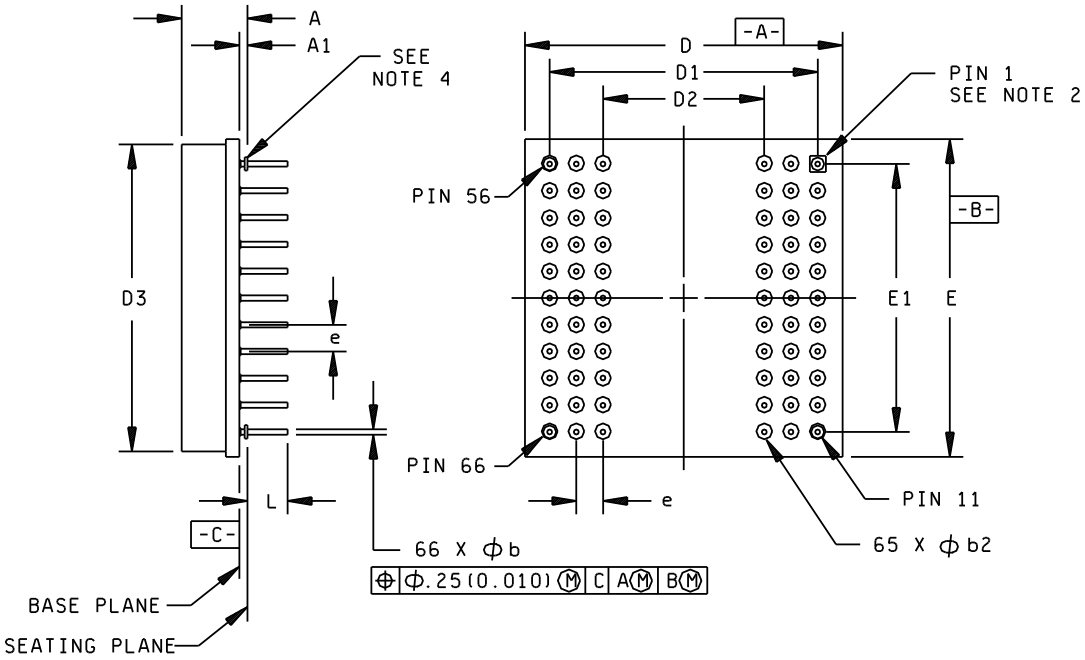


FIGURE 1. Case outlines - continued.

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.94	6.22	0.130	0.245
A1	0.75	0.77	0.005	0.035
⌀b	0.41	0.51	0.016	0.020
⌀b2	1.65	1.91	0.065	0.075
D/E	26.92	30.48	1.060	1.200
D1/E1	25.40 BSC		1.000 BSC	
D2	15.24 BSC.		0.606 BSC	
D3	26.16	34.29	1.030	1.350
e	2.54 BSC		0.100 BSC	
L	3.68	3.94	0.145	0.155

NOTES:
1. The U.S. preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Pin 1 is identified by 0.070 square pad.
3. Pin numbers are for reference only.
4. Case outline U has standoffs and case outline X does not have standoffs.
5. For case outline U, dimension A is measured from the top of the package to the bottom of the standoff. For case outline X, dimension A is maesured from the top of the package to the bottom of the seating plane.
6. For case outline U, dimension L is measured from the bottom of the standoff to the end of the lead. For case outline X, dimension L is measured from the bottom of seating plane to the end of the lead.

FIGURE 1. Case outlines - Continued.

Device types	All	Device types	All	Device types	All	Device types	All
Case outline	M	Case outline	M	Case outline	M	Case outline	M
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS3}$	19	I/O8	36	$\overline{CS2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CS1}$	51	I/O24	68	$\overline{CS4}$

FIGURE 2. Terminal connections

Device types	All	Device types	All	Device types	All	Device types	All
Case outlines	N,T	Case outlines	N,T	Case outlines	N,T	Case outlines	N,T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CS1}$	19	I/O8	36	$\overline{CS4}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V_{CC}	44	I/O31	61	V_{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE}$
17	I/O7	34	$\overline{CS2}$	51	I/O24	68	$\overline{CS3}$

FIGURE 2. Terminal connections - continued.

Device type	All	Device type	All	Device type	All	Device type	All
Case outlines	U and X	Case outlines	U and X	Case outlines	U and X	Case outlines	U and X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	I/O8	18	A15	35	I/O25	52	$\overline{WE3}$
2	I/O9	19	V_{CC}	36	I/O26	53	$\overline{CS3}$
3	I/O10	20	$\overline{CS1}$	37	A7	54	GND
4	A14	21	NC	38	A12	55	I/O19
5	A16	22	I/03	39	NC	56	I/O31
6	A11	23	I/015	40	A13	57	I/O30
7	A0	24	I/O14	41	A8	58	I/O29
8	A18	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A1
10	I/O1	27	$\overline{OE}$	44	I/O18	61	A2
11	I/O2	28	A17	45	V_{CC}	62	A3
12	$\overline{WE2}$	29	$\overline{WE1}$	46	$\overline{CS4}$	63	I/O23
13	$\overline{CS2}$	30	I/O7	47	$\overline{WE4}$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A4	66	I/O20
16	A10	33	I/O4	50	A5		
17	A9	34	I/O24	51	A6		

FIGURE 2. Terminal connections - continued.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	MODE
V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Read
V_{IH}	X	X	High Z	Standby
V_{IL}	V_{IH}	V_{IH}	High Z	Output disable
V_{IL}	V_{IH}	V_{IL}	D_{IN}	Write

Notes:

1. V_{IH} = High Logic Level
2. V_{IL} = Low Logic Level
3. X = Do not care (either high or low)
4. High Z = High Impedance State

FIGURE 3. Truth table.

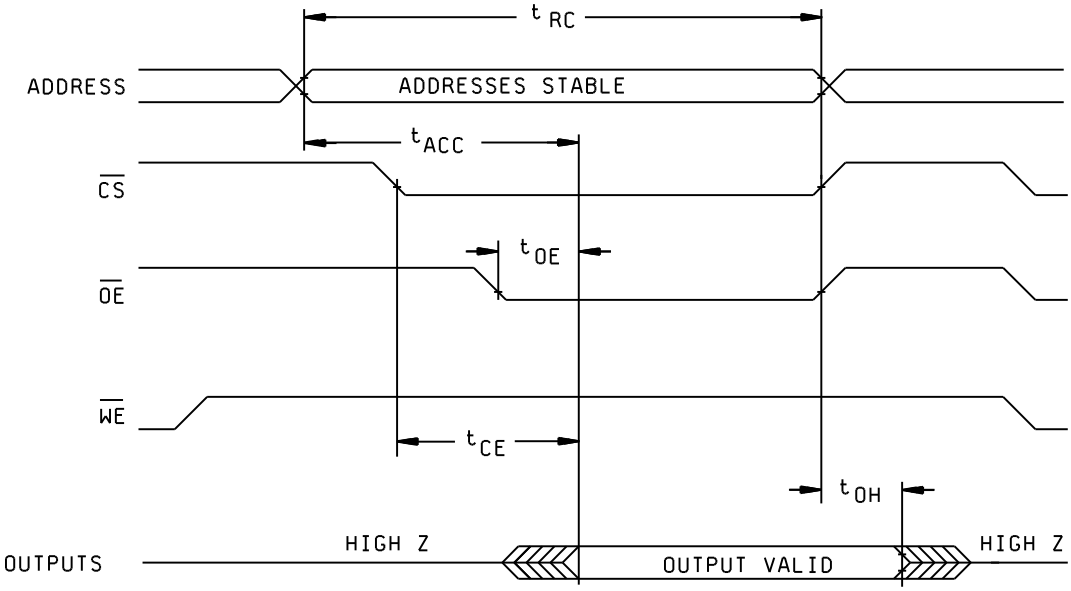


FIGURE 4. Read cycle timing diagram.

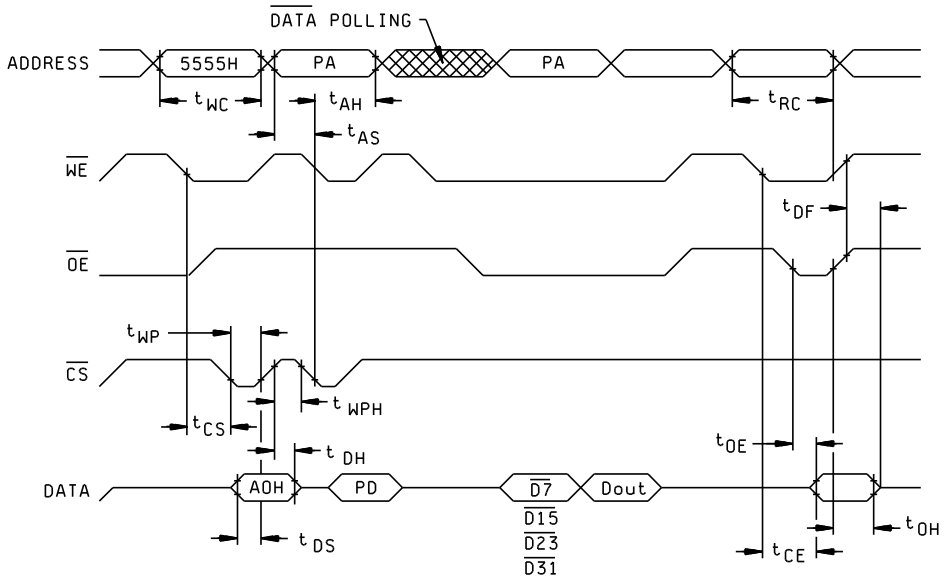


FIGURE 5. Write/Erase/Program operations, WE controlled.

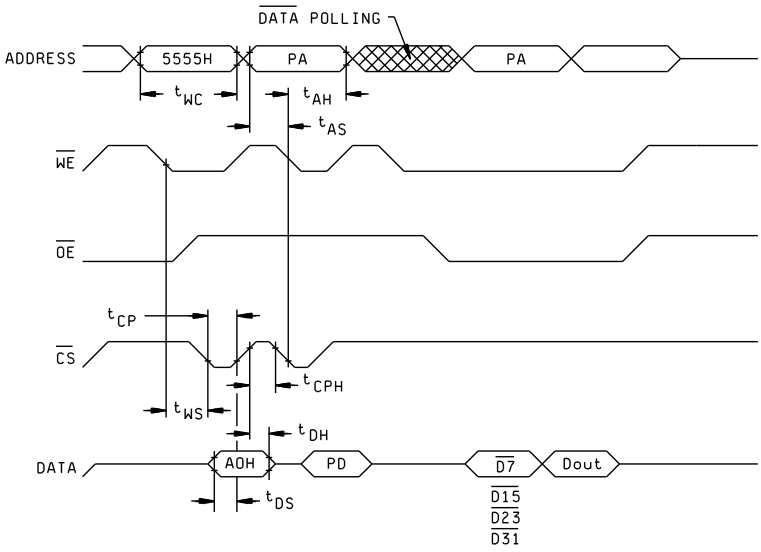


FIGURE 5. Write/Erase/Program operations, CS controlled.

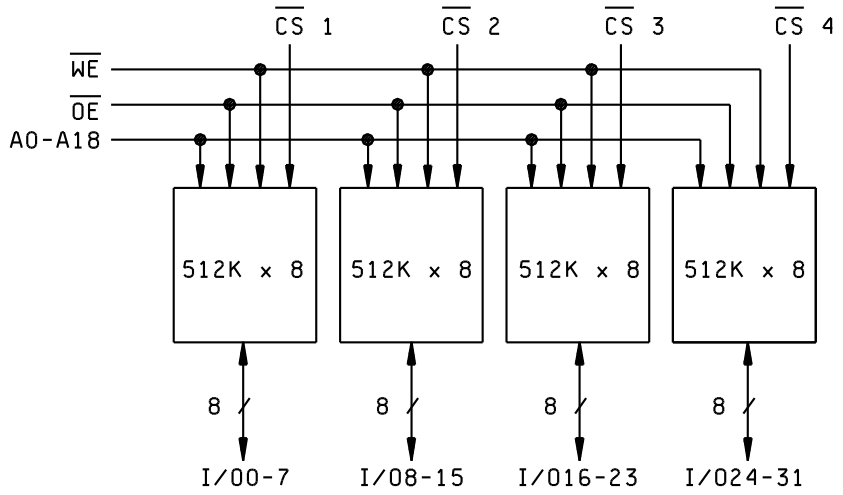


FIGURE 6. Block diagram, Case outlines N and T.

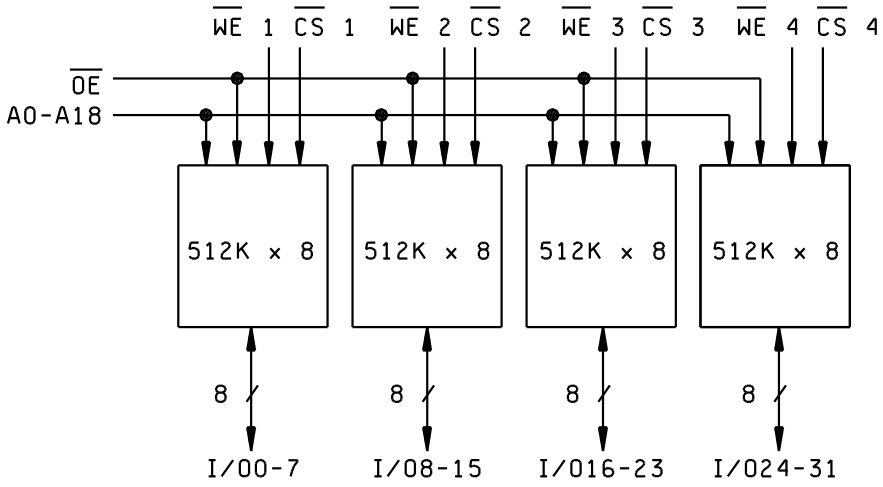
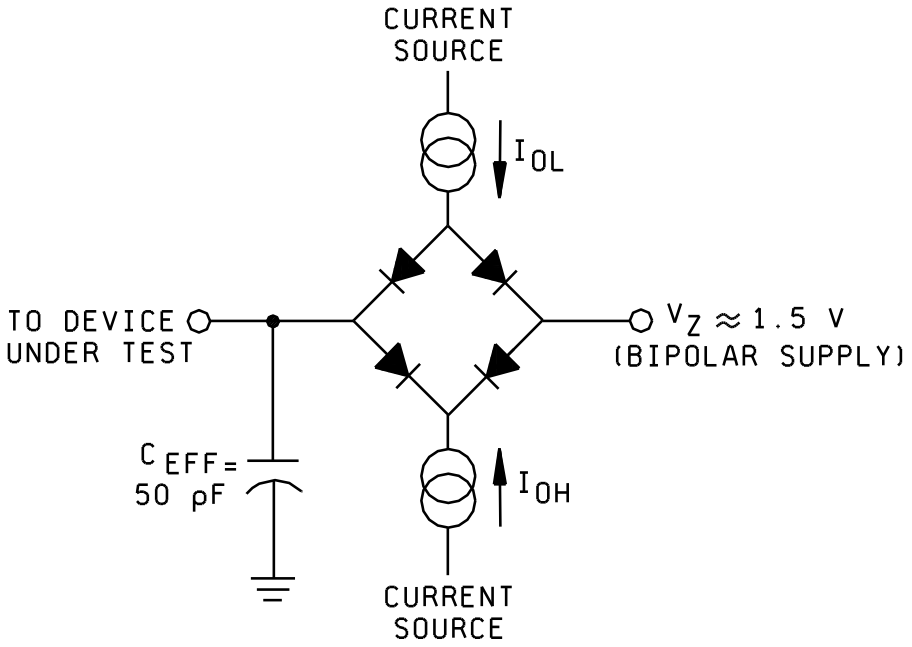


FIGURE 6. Block diagram, Case outlines M, U, and X.



Parameter	Typ.	Unit
Input Pulse Level	0 - 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Load Capacitance	50	pf

Notes:
1. V_Z is programmable from +2V to +7V
2. I_{OL} and I_{OH} are programmable from 0 to 16 mA.
3. Tester impedance is Z_0 = 75 ohms.
4. V_Z is typically the midpoint of V_{OL} and V_{OH}.
5. I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.
6. ATE tester includes jig capacitance.

FIGURE 7. Output load circuit.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	1,4,7,9
Final electrical test parameters	1*,2,3,4,7,8A,8B,9,10 11
Group A test requirements	1,2,3,4,7,8A,8B,9,10, 11
Group C end-point electrical parameters	1,2,3,4,7,8A,8B,9,10 11
MIL-STD-883, group E end-point electrical parameters for RHA devices	Subgroups** (in accordance with method 5005, group A test table)

* PDA applies to subgroup 1.
** When applicable to this standard microcircuit drawing, the subgroups shall be defined.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection. Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table on figure 3.

4.3.2 Group B inspection. Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection. Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition B. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection. Group D inspection shall be in accordance with MIL-PRF-38534.

4.3.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). See MIL-PRF-38534 to perform inspection.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0526.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0676.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-PRF-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-PRF-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply for device classes H and K. Sources of supply for device classes H and K are listed in QML-38534. The vendors listed in QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 96-07-31

Approved sources of supply for SMD 5962-94612 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Standard 1/ Microcircuit Drawing PIN	Vendor CAGE number	Vendor similar PIN 2/
5962-9461201HMX	54230	WF512K32-150G2Q5
5962-9461201HMX	88379	ACT-F512K32N-150F5Q
5962-9461201HNC	54230	WF512K32F-150G4Q5
5962-9461201HTC	54230	WF512K32-150G4TQ5
5962-9461201HUX	54230	WF512K32N-150HQ5
5962-9461201HUX	88379	ACT-F512K32N-150P7Q
5962-9461201HXX	88379	ACT-F512K32N-150P3Q
5962-9461202HMX	54230	WF512K32-120G2Q5
5962-9461202HMX	88379	ACT-F512K32N-120F5Q
5962-9461202HNC	54230	WF512K32F-120G4Q5
5962-9461202HTC	54230	WF512K32-120G4TQ5
5962-9461202HUX	54230	WF512K32N-120HQ5
5962-9461202HUX	88379	ACT-F512K32N-120P7Q
5962-9461202HXX	88379	ACT-F512K32N-120P3Q
5962-9461203HMX	54230	WF512K32-90G2Q5
5962-9461203HMX	88379	ACT-F512K32N-090F5Q
5962-9461203HNC	54230	WF512K32F-90G4Q5
5962-9461203HTC	54230	WF512K32-90G4TQ5
5962-9461203HUX	54230	WF512K32N-90HQ5
5962-9461203HUX	88379	ACT-F512K32N-090P7Q
5962-9461203HXX	88379	ACT-F512K32N-090P3Q
5962-9461204HMX	54230	WF512K32-70G2Q5
5962-9461204HMX	88379	ACT-F512K32N-070F5Q
5962-9461204HNC	54230	WF512K32F-70G4Q5
5962-9461204HTC	54230	WF512K32-70G4TQ5
5962-9461204HUX	54230	WF512K32N-70HQ5
5962-9461204HUX	88379	ACT-F512K32N-070P7Q
5962-9461204HXX	88379	ACT-F512K32N-070P3Q

1/ Parts that are listed with lead finish designator X are available in lead finishes A or C.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN - CONTINUED.

DATE: 96-07-31

Approved sources of supply for SMD 5962-94612 are listed below for immediate acquisition only and shall be added to QML-38534 during the next revision. QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of QML-38534.

Vendor CAGE number	Vendor name and address
54230	White Microelectronics 4246 East Wood Street Phoenix, Az 85040-1991
88379	Aeroflex Circuit Technology Corporation 35 South Service Road Plainview NY, 11803